Manufacturing and Test

By Hem Hingarh, VP Engineering, Synapse Design

Technology Trends

Process technology is progressing at a very fast pace and 16/14nm FinFET- based SOCs are available from various fabless companies. Significant investments in the development of advanced technology nodes are being made to ensure that future demands are met. This makes fab utilization of primary importance. To that end, SOC companies are accelerating the introduction of highly integrated products in these process technologies.

Custom SOCs designed for consumer applications and powered mostly by battery, must possess low active and stand-by power characteristics. FinFet (16/14nm) devices provide significant reduction in static leakage leading to lower power and high drive currents which in turn enable faster switching at lower supply voltages. Application of these process technologies is ideal for this application space.

For the first time, there is a fundamental change to the structure of the transistor (3D) resulting in new defect mechanisms creating a major challenge on the SOC design and manufacturing. In particular, FinFET critical dimensions are, for the first time, significantly smaller than the underlying node dimensions, leading to an increase in the number and complexity of layout and circuit-sensitive defects. This also means greater variability from design to design, making yield an ongoing challenge even as the process matures. New test structures and technology bring-up methodologies are necessary to control process induced variations while layout and circuit design needs to be optimized to mitigate this process impact.

DFT / DFM

It is important that both foundries and SOC design teams work together to better understand defects that could affect product

quality and yield. There is a critical feedback loop that comes from yield information physical defect analysis. This data drives updates to DFM rules. Foundries have also identified that FinFET based memories have many new defect types, each categorized as a unique fault model. It's critical to develop an optimized suite of test algorithms that detect these defects while keeping test cost low.

Jointly (fab and fabless design customer) driven DFX methodologies are being used to accelerate technology bring up and are now enabling customers fast volume ramp up.

DFT – Testability and Yield Improvement

At a high level, increasing SOC sizes including processors (>100Mgates), memories (100-200Mb), system interfaces, mixed signal blocks, various IPs and complex packaging have made SOC tests a tough challenge.

Designers have to consider various manufacturing related issues including DFT: How the IPs and other design blocks will be controllable and observable at top level; design for debug; yield ramp; and how the entire SOC can be tested without increasing test time and overall test cost.

In addition to reducing test cost, companies must focus on yield improvement, improve product quality and lower DPPM, in order to address the need to keep track of data for all phases of manufacturing.

In addition to DFT, DFM, DFY (Design for Yield), designers should consider the following issues:

- Concurrent test of IPs, its impact on power dissipation
- Device performance & power tuning like DVFS during test
- Increasing test vector generation – for manufacturing test, characterization test, acceptance/quality test

- Increasing size of test vectors – impact on test time
- Maintaining Die/ package traceability
- Data collection and data analysis, defect identification and yield improvement

Trends in Testability features

Advanced DFT methodologies are used to design and test special structures to enable fast failure analysis identifying design and manufacturing defects.

System and RTL design must include DFT features to meet design requirements such as: Impact of DFT on PPA (test power, test performance and test area overhead); testability coverage goals including stuck-at faults, transition faults and at-speed defects; automatic test pattern generation (ATPG) vectors; and test time.

Most SOCs use multi-power islands, DFT design has to be power domain-aware and construct scan chains appropriately leveraging industry standard power specifications like (UPF/CPF).

DFT IP like JTAG boundary scan, memory BIST collars, logic BIST (LBIST) and compression macros are readily integrated into the design and verified during the logic design process. BIST adoption is evolving beyond embedded memories to logic and mixed-signal blocks. In addition, adding test structures on chip enables greater test efficiency through increased test parallelization.

SOC designs must provide the capability to enable on-die circuitry (BIST, Logic DFT, etc.) and include design and test special structures to enable fast failure analysis identifying design and manufacturing defects. In the past, it was sufficient to identify failing bit and logic gate for yield improvement; however, in today's environment we need to be able to isolate faulty blocks and replace with spares and even tune the performance.

DFT provides additional value for expensive on-chip test functions by using an external tester. By combining DFT solutions for an on-chip and off-chip tester strategy, we can improve speed test coverage. If designed properly, testing at speed or at multiple speeds, can be performed without the need for an external add-on hardware on tester. It also reduces the time-to-market window, while ensuring superior quality SoC designs and reduced testing costs.

Testability features continue to evolve to address the increased complexity of SoC and 14/16 nm FinFet process technologies requiring new fault models and identification of leaky power switches. With new technologies, whether in the form of new circuit design, a new algorithm or new IP modules, the EDA tools are being updated.