Low-Power SOC Design Integration Issues

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As technology evolves, more functionality is being added on SOCs. At same time, pressure is building up to reduce operating and standby power. Today the market is focused on reducing power in wide spectrum of SOCs from CPUs, GPUs and Mobile not just IOT/wearable SOCs. Battery powered SOCs require much more aggressive power reduction techniques. All of these SOCs today have a large number of power and clock domains and they have hundreds of IPs and memories.

These types of multi-power domain SOCs are complex and present new integration challenges because many blocks have different operating modes at different voltages, different clock period and duty cycles of each block being awake, asleep or in shutdown mode. We must pay more attention to applications that dictate modes of operations, power and battery life requirements.

While power gating and other techniques are effective today, these techniques may not be enough for many IOT low-power SOCs. We have to think in terms of design-for- power in terms of energy consumptions at all levels of design including overall system/ application, architectural, power management, RTL, DFT, and physical implementation in addition to technology and process advancements.

Power management units (PMU), a mixed signal block and digital controller are very important blocks of a low power SOC. In addition to power gate digital block with a switch, but for battery powered designs it is possible to power gate the analog portions. In these designs, it is important to deal with issues such as stability and the time necessary to reach a stable state. This requires an analog circuit designer and has to be done much more carefully than for digital design.

Success with multi-voltage SOCs requires careful planning and a robust methodology and toolset for all stages of the implementation. Let us look at key aspects of methodology which works and what need upgrades. One need proper tools for the analog and digital part and you need to be conscious of your flow.

System Requirements & RTL development

A detailed requirement document is needed, including: Always-on (AON) block; power domains; power gating; clocking; system level and block level power options with timing; and a description of how power domains interact with each other. This information is used by firmware/software RTL designers and by verification and physical implementation teams. Also, one must define power or ground switches for each domain. There may be a required sequence for powering up the design in order to avoid deadlock.

Also we need an explicit power sequence for each of the power domains to come up

in a well-defined order that assures correct function. And in fact, some IP may require a specific power up sequence. Companies have front-end tools and flows to capture power intent using UPF/CPF including Power State Tables (PST) to define all possible power state combinations; the PST captures the valid interaction between the different power domains so that tools can determine the optimal buffering strategy.

Tools are being developed to address power at the RTL level. This will help identify coarse & fine grain power reduction methods for implementation. The power intent UPF is described at RTL for the logic design. The UPF file is updated during the synthesis flow, and updated again during the place and route process.

Verification

Verification of Power-Intent (UPF/ CPF) using these fine-grained techniques requires close interaction between the verification team, System designer, RTL designers and circuit/ physical implementation team members. In battery powered SOCs, all low level assumptions such as intermittent on/off timing have to be verified at the RTL level and in some cases, must use circuit simulations. Automated solutions are not satisfactory since the analysis must cross all phases - RTL design, Synthesis, and dynamic operation. The addition of low-power mode with multiple power domains creates corner cases that are not detected in functional simulations. This is where formal approach is the one way to ensure their DUT will be free of bugs, as well as unwanted 'Xs.'

Detailed SPICE simulation of the whole chip is not a viable option for these SoCs. Simulation times would be unreasonably increased due to the complexity of power controller block. A detailed simulation of this block would require cycling through multiple power transitions, which in turn requires carefully chosen input vectors for each stage of the design, exponentially increasing simulation times.

Power Domain Verification

This is a critical step to ensure that the power constraints are defined properly and to avoid later surprises. Power-on/ off is a complex issue because analog blocks require technology-dependent stabilization and lock times order tens of milliseconds. Additionally, all power domains have their own reset sequence and timing associated with that.

In particular, we need to make sure that all power domains are completely powered up before issuing reset. Also, the CPU/controller may need to wait until the rest of the chip is powered up before booting.

Use of Formal Tools

Functional Verification of power sequencing is timing consuming and add to schedule. This is one task where formal verification tools will help. Formal tools (MVRC or Jasper/ Cadence) can be used for verifying properties that simulation will take long time to verify such as reset time of all blocks. Formal tool help determine

the logic path that takes the longest time to reset.

Physical implementation
UPF/ CPF based power – intent implementation flow is well established for netlist updates which include insertion of level shifters, Isolation cells etc.

Clock tree Synthesis
The clock tree synthesis engine should use the PST-based buffering solution while expanding the clock tree network across different power domains means that they have to go through level shifters. the clock tree synthesis tools will automatically insert level shifters at the appropriate places. As a general guideline all clock sources reside in always-on blocks as it is tricky to balance skew through level-shifters.

Floorplanning, power grid planning: Multiple power domains require very careful and detailed power grid planning. The power grids become more complex.

Static Timing Analysis
Multi-level voltage scaling presents a greater challenge. The questions is: which multi-corner, multi- mode voltage library to use for synthesis, place and route, and STA?

With multiple voltage, libraries may not be characterized at the exact voltage we are using, timing analysis becomes much more complex. The end result is that the design should meet timing and power requirements for all the mode/corner scenarios.

Designers must ensure that the correct level shifters, retention cells, and other design elements have been accurately placed for each of the different power domains, also verify bulk and well connections at the transistor level. There are tools from EDA companies help automate these checks.

Low Power SOC Issues
There are many design methodology issues requiring automation, but today these are resolved using custom script or manual intervention.

Rush current management
In multi- Voltage domain designs, blocks are powered thru on chip switches or from different external voltage pins or on Chip Regulators LDOs. During power up sequence there is a large current peak for short duration which cause voltage drop that could corrupt retention registers. It is very important to reduce peak current, thru decoupling Caps or adding appropriate delay (daisy chaining) in turn-on signals or clocks for these blocks. One have to carefully design size of Switches to reduce voltage drop. Over-size Switch will increase standby leakage power.

Power estimation issues

The biggest gap in our methodology is that we don't have accurate early power consumption estimation at the system partitioning stage. RTL power estimation tools are just starting to be used. There is little data available on correlation of RTL power with measured silicon results and micro- amp level accuracy especially for battery powered SOCs. These types of tools will have high impact on design flow improvement.

Today most of the resources are assigned to verification including Spice simulation for mixed signal blocks, functional and power-intent verification, power-intent timing interaction and power sequencing at chip and blocks level.

Methodologies are being updated to meet demands of low-power multi-voltage designs, and using the latest tools and flow scripts that incorporate best practices can make the difference between taping out the design on time and within specification.